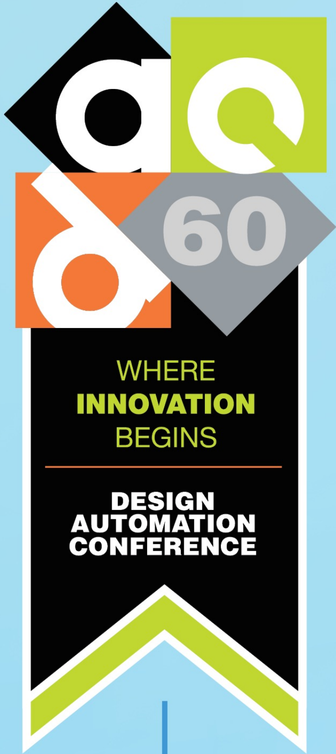
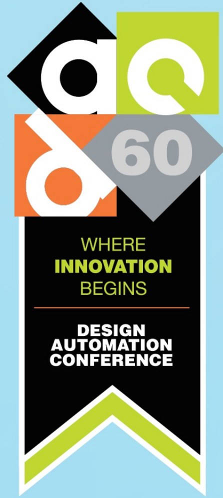


JULY 9–13, 2023

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA



Why is Curvy Design an Opportunity Now?

Moderator: Aki Fujimura, CEO, D2S, Inc.

Panel: John Kibarian, CEO, PDF Solutions

Ezequiel Russell, Sr. Director of Mask Technology, Micron

Andrew Kahng, Professor, UCSD

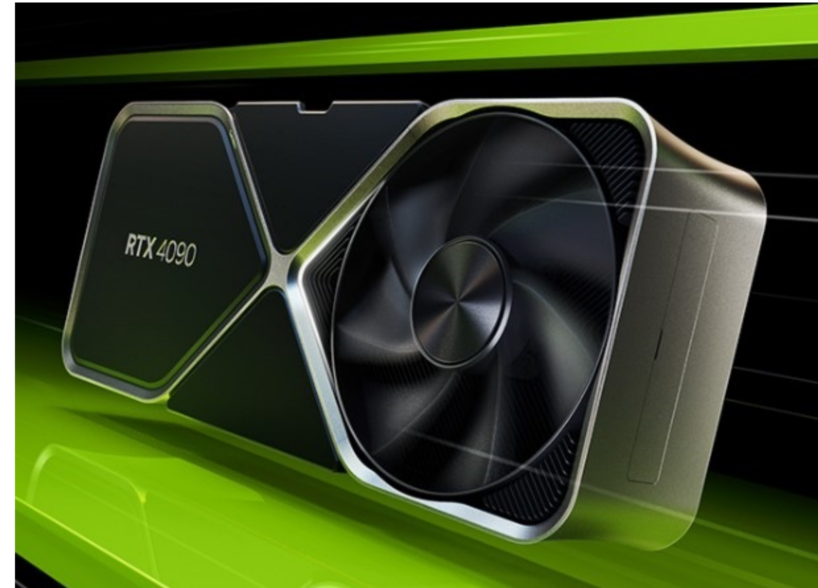
Steve Teig, CEO, Perceive

San Francisco is Ahead of the Curve

Today's GPU Workstation = 43,000 Cray-2s

340,000,000x Price Performance: It's time to rethink EDA

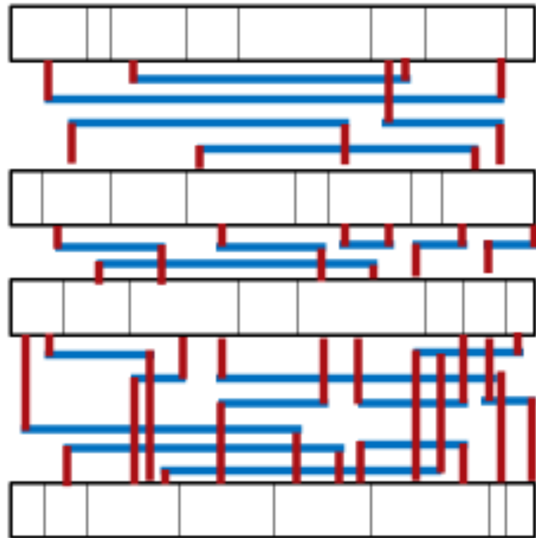
Cray-2 (1985)
1.9 GFLOPS w/500MB @ $15M



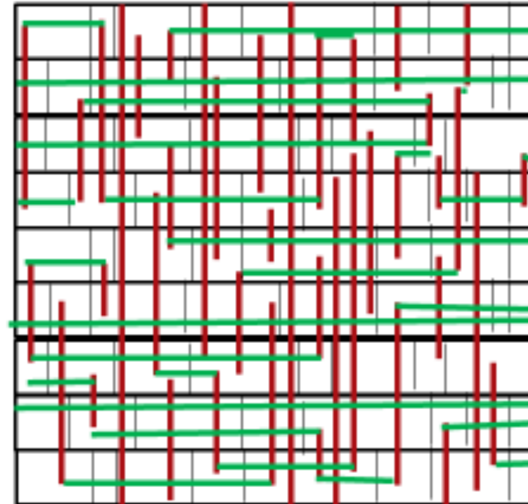
NVIDIA RTX 4090 (2022)
83 TFLOPS w/24GB @ $1,900

Once Upon a Time, Rectangles Served a Purpose

But times (and computing) have changed...

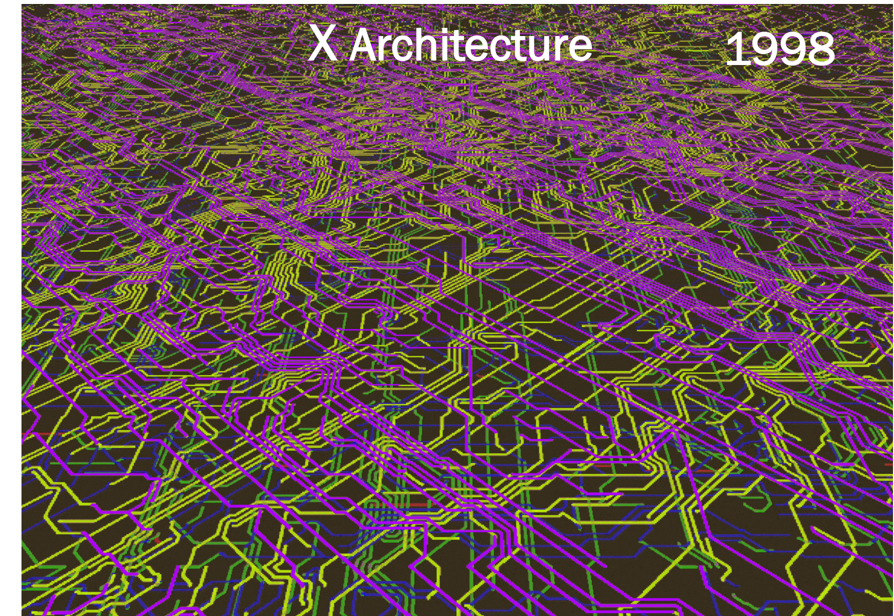


1987



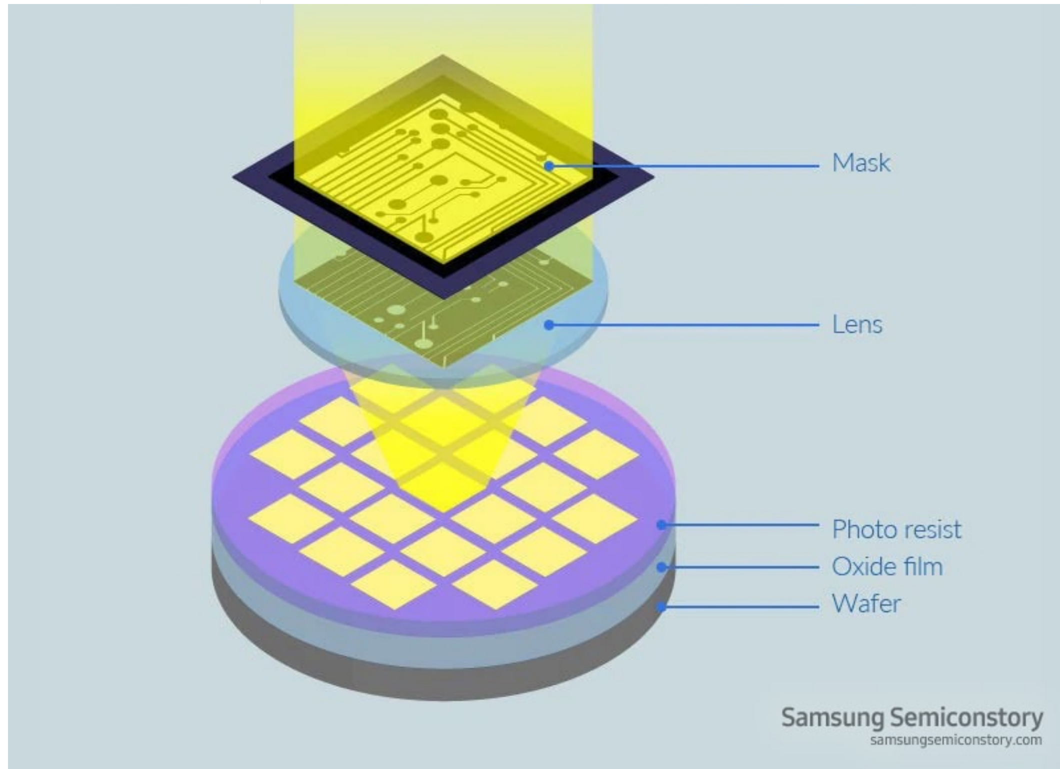
Source: Tangent

DEF, LEF, ECO, ...



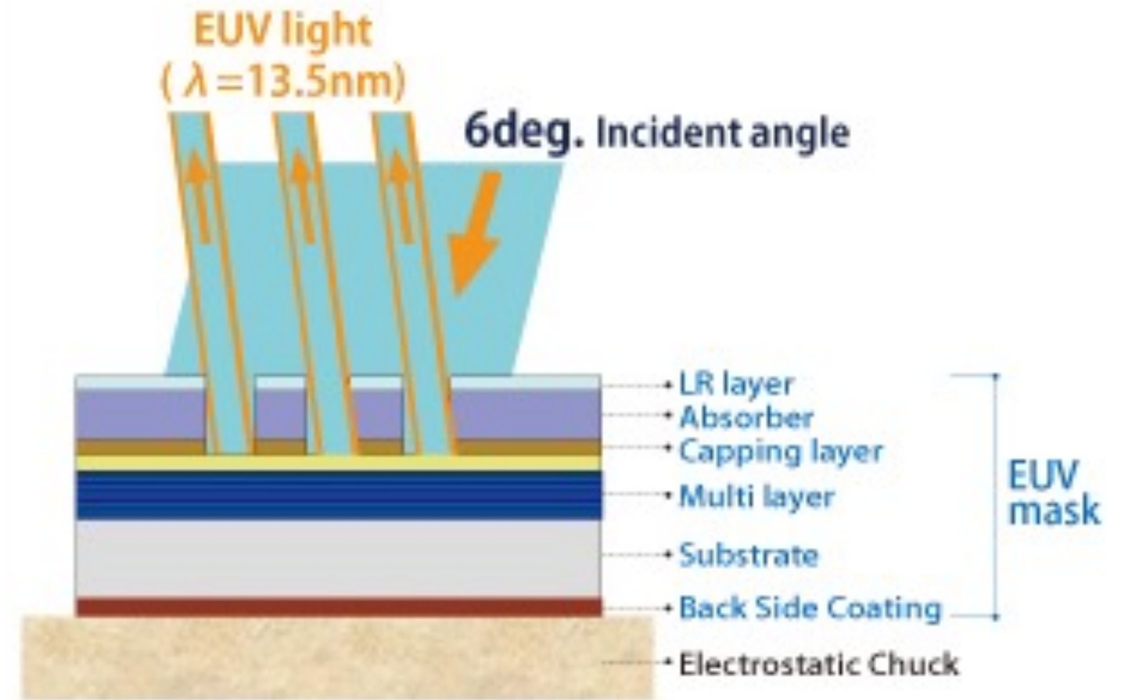
Source: Simplex

Wafers are Exposed by Masks (EUV, too!)



Source: Samsung

193i



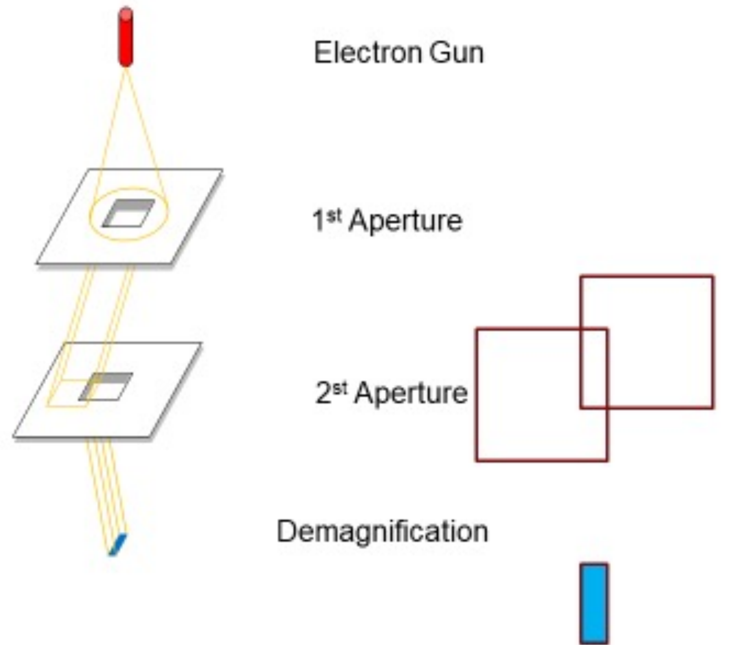
Source: ASML

EUV

Leading Edge is 100% Multi-beam Mask Writers

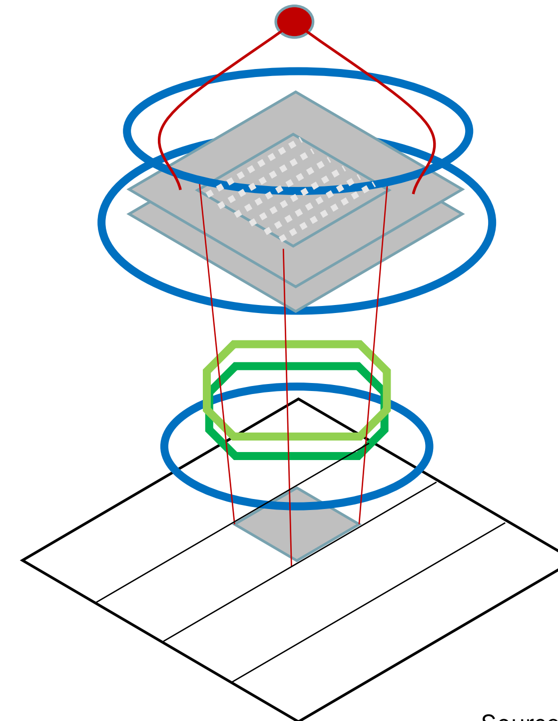
Multi-beam write-time is independent of shape: Curvilinear (curvy) masks have been enabled

Before : Variable-Shaped Beam



Source: NuFlare

Now : Multi-beam Mask Writers

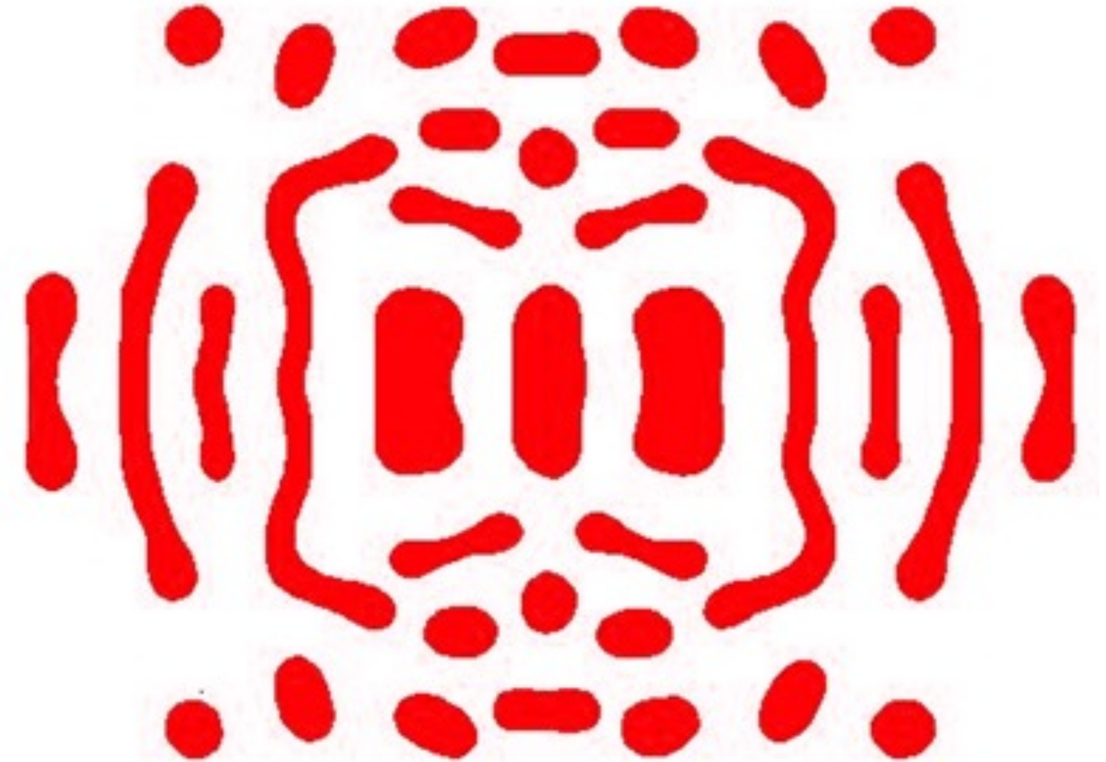


Source: NuFlare

ILT is Software that Computes Mask Shapes

Generates Curvy Masks for Multi-beam Writing

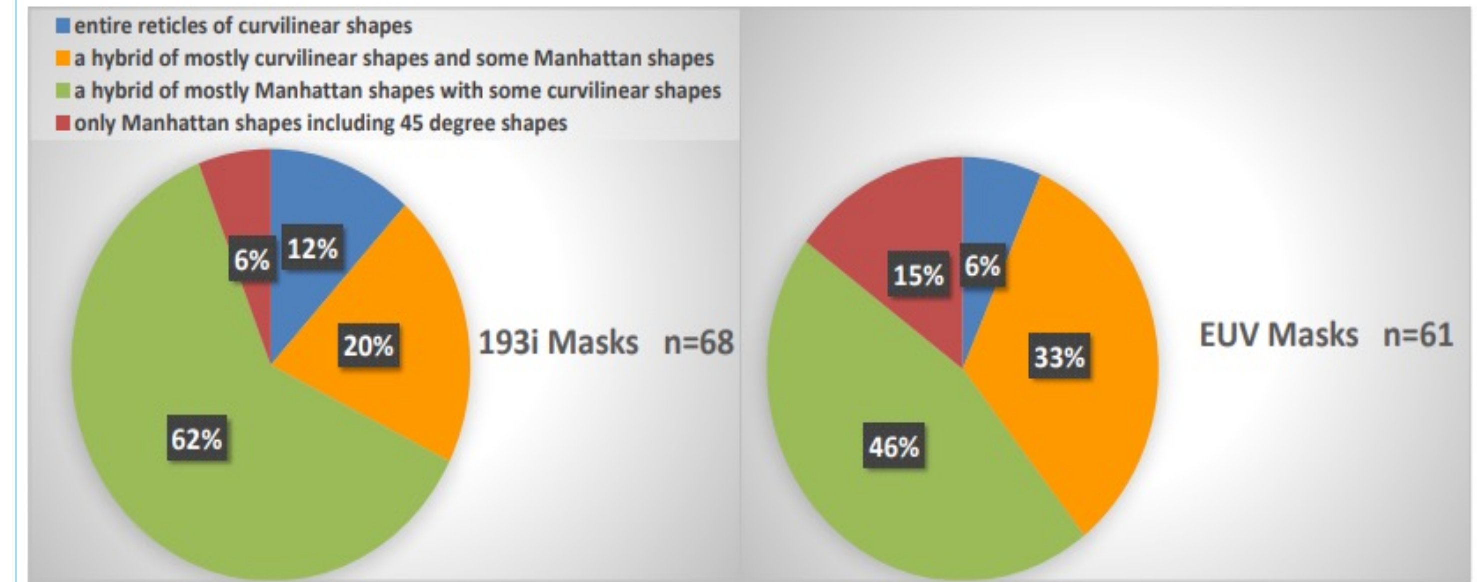
Design (Wafer Target)



Curvilinear ILT (Mask Target)

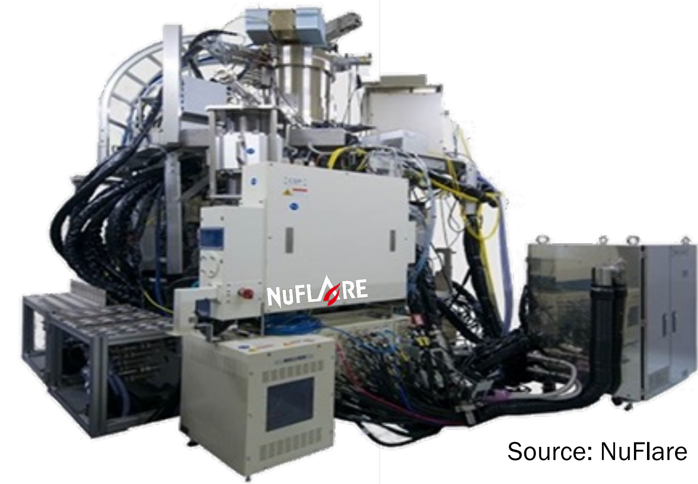
Both 193i and EUV Will Use Curvy Masks

- Masks are written by data
- Wafers are written by masks
- Before: Manhattan
  - Some 45-degree triangles
- Now: Curvy Masks
  - Just as accurately
  - Just as quickly
  - For the same cost



eBeam Initiative Luminaries Survey, ebeam.org

Curvy Wafer Targets Can Be Manufactured Now

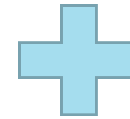


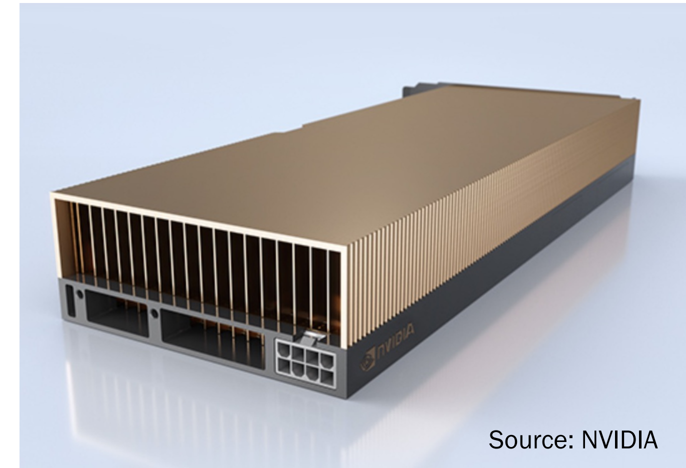
Source: NuFlare

Multi-beam Mask Writer

Curvy ILT

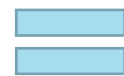
Source: D2S

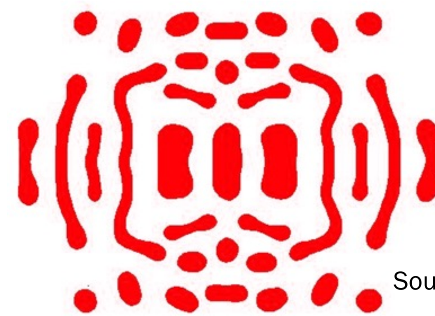




Source: NVIDIA

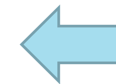
GPU Acceleration

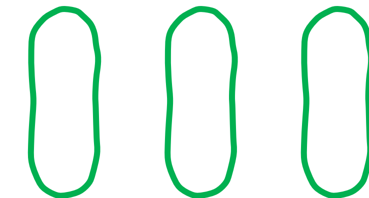




Source: D2S

Curvy Masks





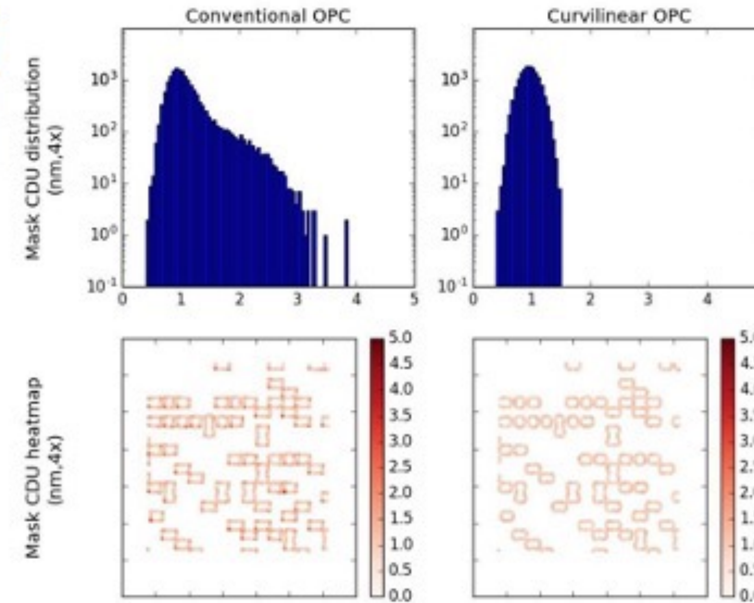
Design (Wafer Target)

"Ask for what you want!" – Ryan Pearman, Intel

True for Wafer Targets too!

Curvilinear Mask Variability is 2.5x Better

Mask EPEU (nm, 10, 4x)	Conventional OPC	Curvilinear OPC	
50%	1.01	0.96	95%
max	3.82	1.49	39%



Pearman, 12495-19 intel. 1

Curvilinear OPC Output is Required

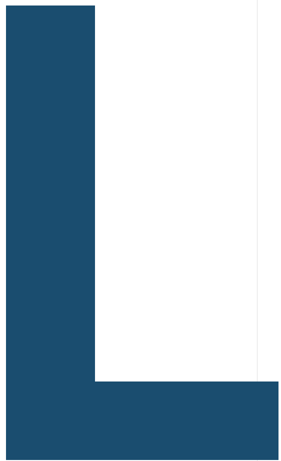
- It is Better to Ask for Manufacturable Masks
  - The mask shop can make the exact mask litho requests (better fidelity)
  - We remove a lot of complexity in the computational lithography
  - Need EDA vendors to constrain the OPC output to manufacturable shapes
- Curvilinear OPC has Better Mask CDU
  - The mask has >2.5x less worst case variability
- Curvilinear OPC is One Step on EPE Reduction
  - Curvature constrained OPC still gives a better resist level solution
  - Curvilinear OPC contributes 0.25nm of random error reduction

SPIE Advanced Lithography 2023 Pearman, 12495-19 intel. 34

Source: Pearman, et al, Intel, "A CD Uniformity study comparing MRC-constrained Manhattan to Curvilinear OPC corrections on EUV", SPIE AL 2023, 12495-19

"Curvy Design" Means Curvy Connections

Manufacturable Shapes are More Reliable



Manhattan Design

Non-Manhattan Design

Curvy but
Not Curvy Design

Unachievable Wafer Targets

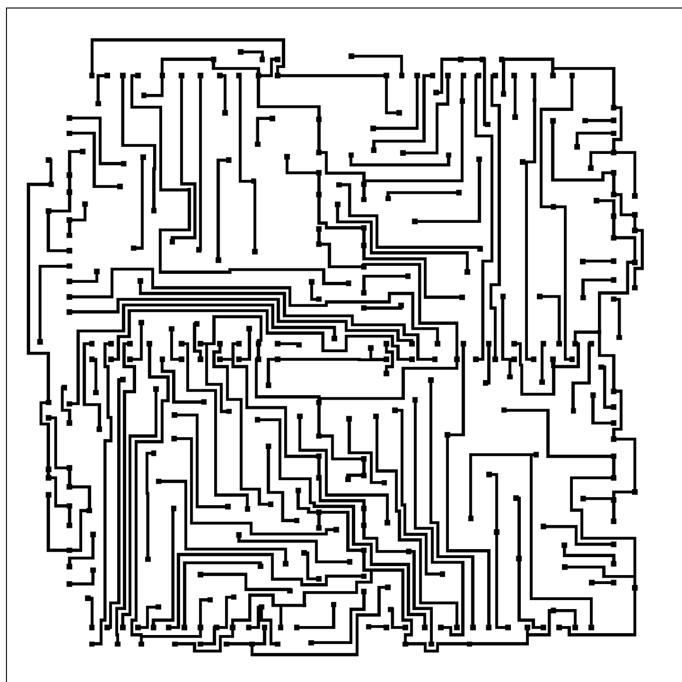
Curvy Design

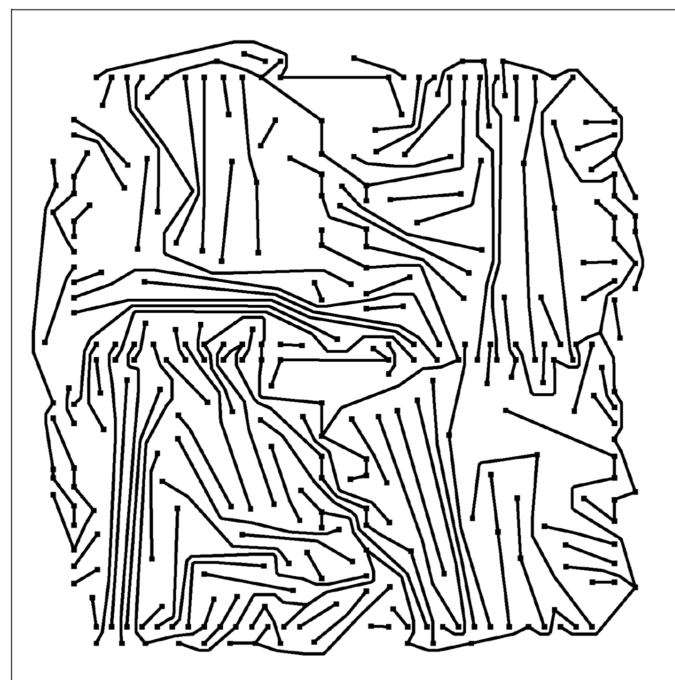
Curvy Design

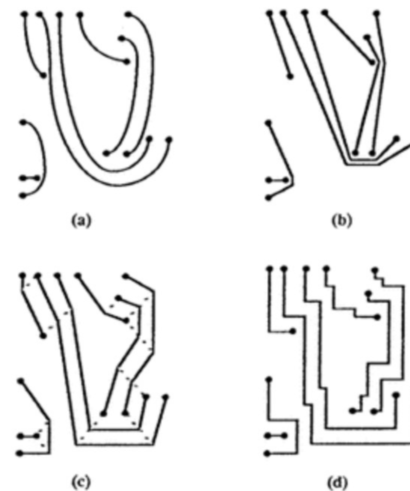
Manufacturable Wafer Targets

Dai-Dayan Rubber Band Routing

Any angle-routing >30% avg via reduction: manufacturable now


Conventional Routing

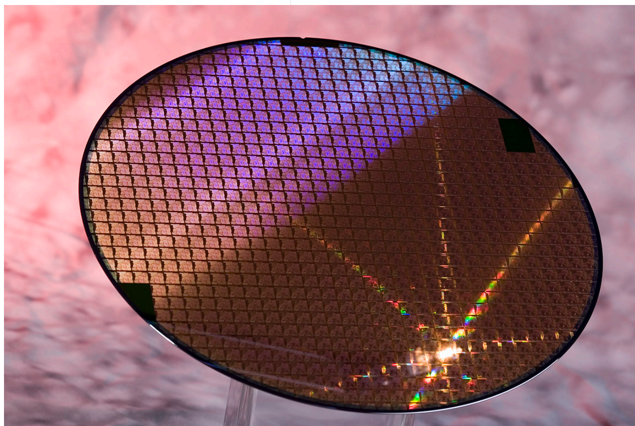

Euclidean Routing

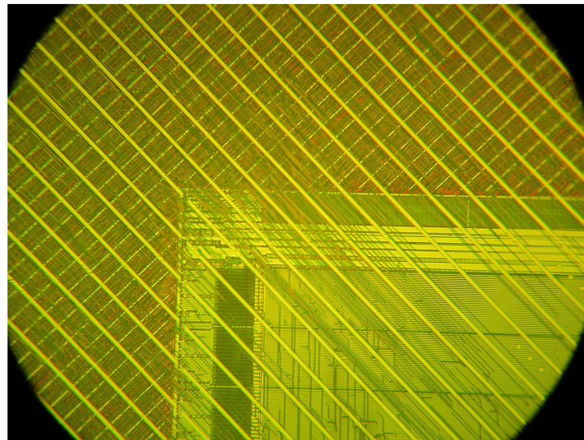


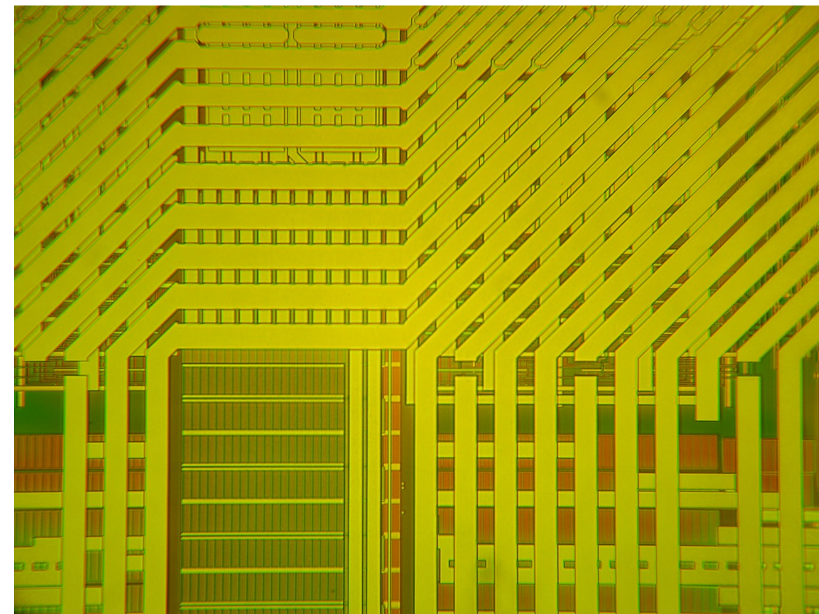
Example	Improvement	
Name	Len%	Vias%
APEX/01	1.16	38.24
APEX/02	1.03	43.10
APEX/03	-1.20	34.16
DS15/01	-0.44	37.14
DS15/02	1.37	3.85
DS15/03	0.12	66.67
GDX/01	0.42	23.08
GDX/02	0.04	53.85
GDX/03	0.92	12.50
GDX/04	0.72	0.00
Avg	0.41	31.26

Source: Tal Dayan, PhD Dissertation, UC Santa Cruz, 1997

X Architecture Proved
30% Wire Length Reduction







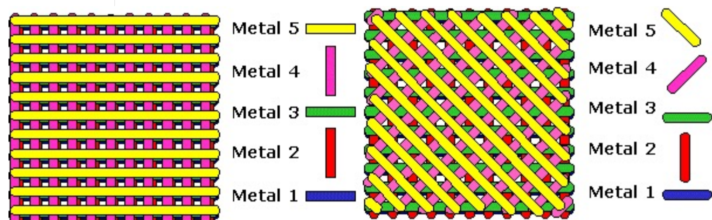
Source: ATi

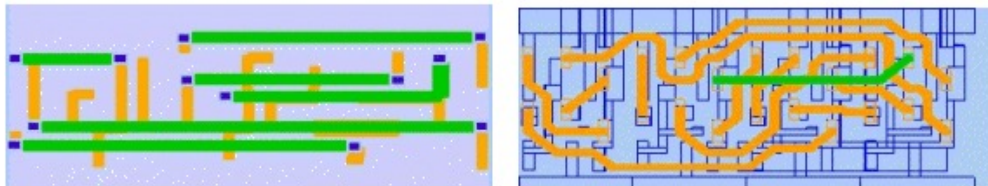
20% Faster Processing Time + 10% Area Reduction

斜め配線が可能な設計手法「X　Ａｒｃｈｉｔｅｃｔｕｒｅ」による初のＬＳＩ設計について

2002年2月6日

従来手法の設計に比べ処理速度２０%向上とチップ面積１０%削減を実現





Source: Toshiba

EDN

NEWS | NEWS ARCHIVE

Agere Leverages X Architecture in 90nm Mobile Chip

EDN JUNE 28, 2006
BY EDN STAFF

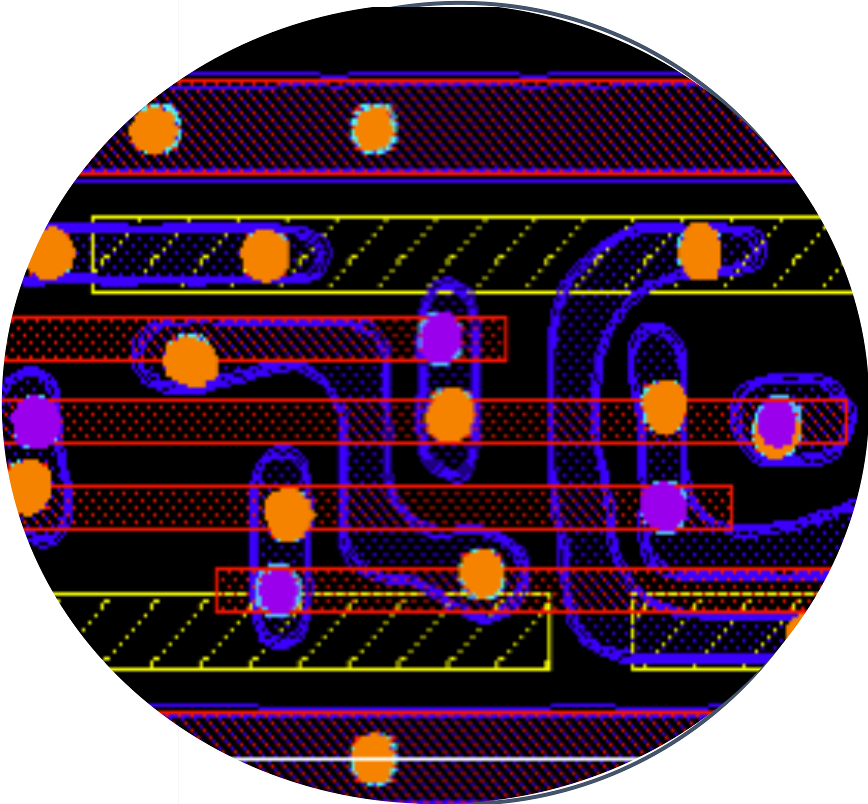
Print PDF Email COMMENTS 0

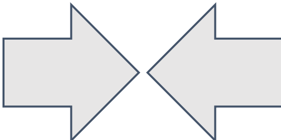
Agere said it was impressed with the die-size reduction and reduced power dissipation resulting from the wirelength reduction achieved with the X Architecture.

Craig Garen, VP of mobility product development with Agere concluded in a statement, “Our company has confirmed that the Cadence X Architecture has realized a wirelength reduction of more than nine meters — approximately 30 percent — versus previously used Manhattan routing in the same technology. The ease with which the Cadence X Architecture integrated into our sign-off flow enabled us to meet our aggressive tape-out schedule.”

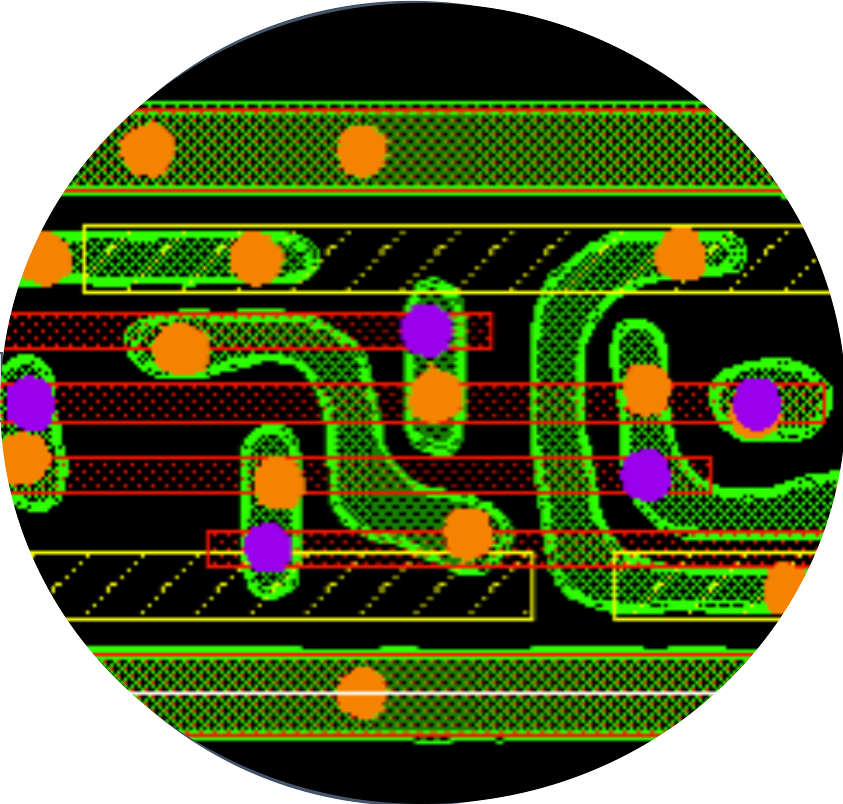
Curvy Future: What You Design is What You Get

Design

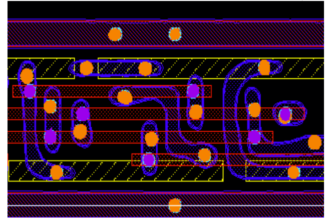




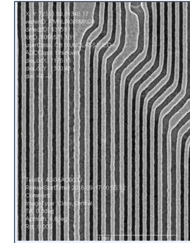
Manufacturing



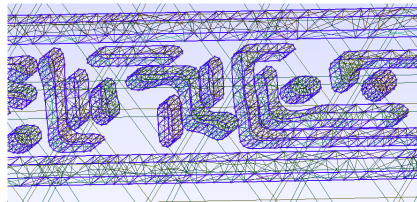
EDA: Four Things Needed to Enable Curvy Design



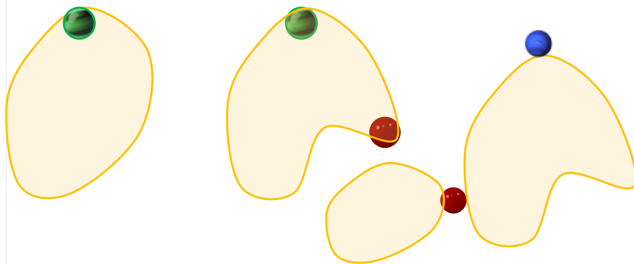
Custom Design



Routing



Parasitic Extraction



DRC

The Debate on Curvy Design

Barriers

- Fabless needs foundry support
- Foundry needs fabless demand
- Tool infrastructure is way too inefficient for curvy design
- Perception that everything in EDA needs to change
- Benefits are unclear/unproven

- Net: It's a big change

Potential Benefits

- Yield
- Power
- Performance
- Area and layer-pair elimination
- Cost

- Reduce vias and wire length
- EUV and non-EUV leading edge

John Kibarian

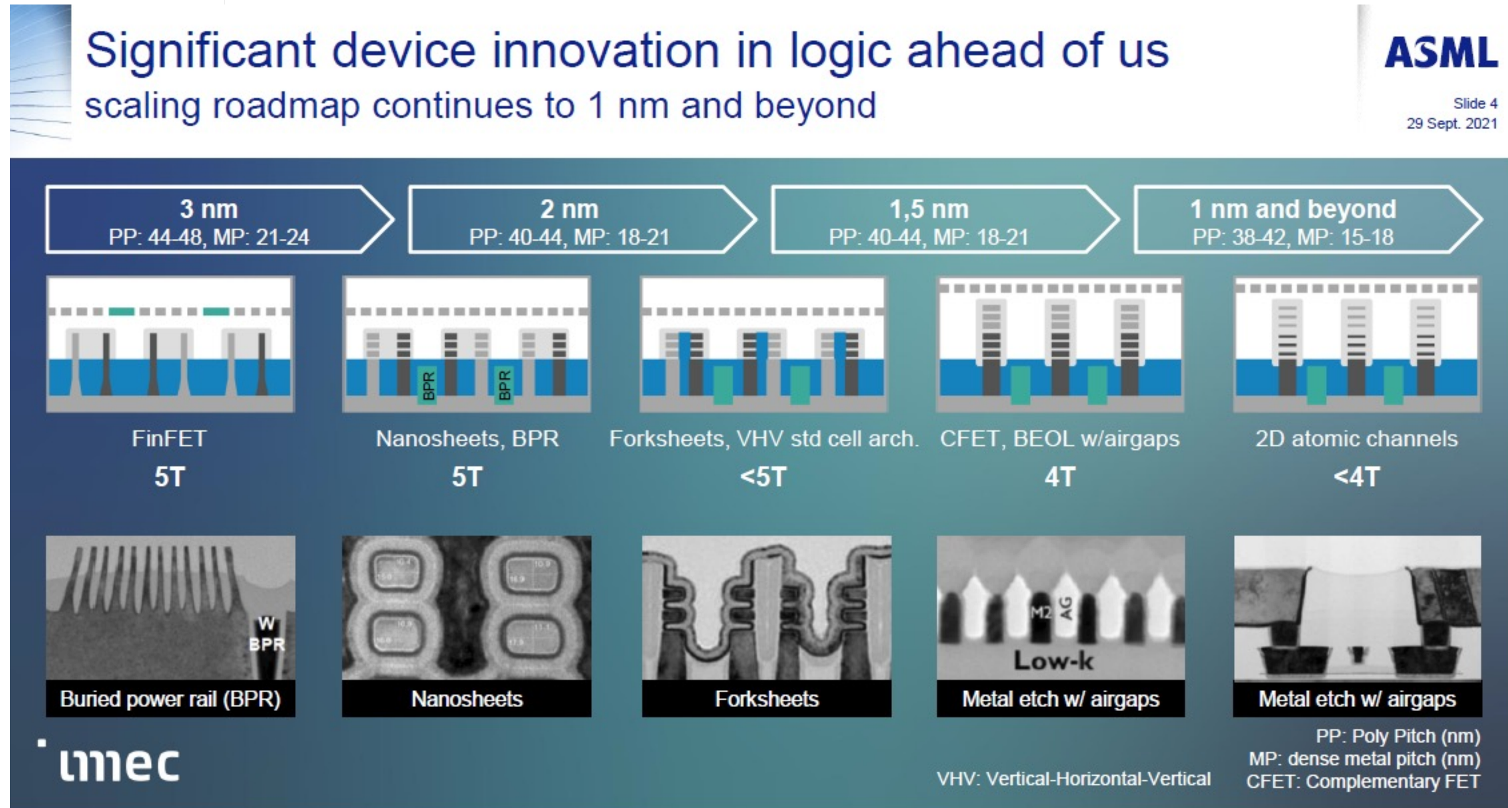
- Founder and CEO, PDF Solutions

  The Yield Management Company
  - Founded 1991
  - Industry-leading data analytics and professional services towards Industry 4.0

- Public company since 2001
  - Current Market Cap of $1.35B

- CMU SEMATECH Center of Rapid Yield Learning

Moore's Law (Pitch scaling) Continues



- Feature scaling is continuing but....
- Metal pitch scales 30% over 4 nodes (when that used to be in 1 node)

While Pitch Scaling Slows, Other Techniques Take Over

Moore's law evolution: the next decade

From cost per transistor through density, to cost of time and energy through systems

ASML

Slide 12
29 Sept. 2021

System Energy Efficient Performance[3] [1/J·s]

Transistor Energy Efficient Performance[2] [[1/J·s]

Transistor density[2] [#/mm²]

Litho density[2] (Contact Poly Pitch*Metal Pitch)[-1] [10^9/mm²]

Clock Frequency[1] [MHz]

4x/2yrs

3x/2yrs

Device and layout optimization

Public data | Customer projection | Speculation

Equivalent Scaling: HKMG, Strained Silicon

New Transistor Structure/Materials: FinFET, EUV, High Mobility, DTCO

1970 1980 1990 2000 2010 2020 2030 2040

Sources: [1]Karl Rupp, [2]ASML data and projection using Rupp, [3]Mark Liu, TSMC, normalized to transistor EEP in 2005.

Public

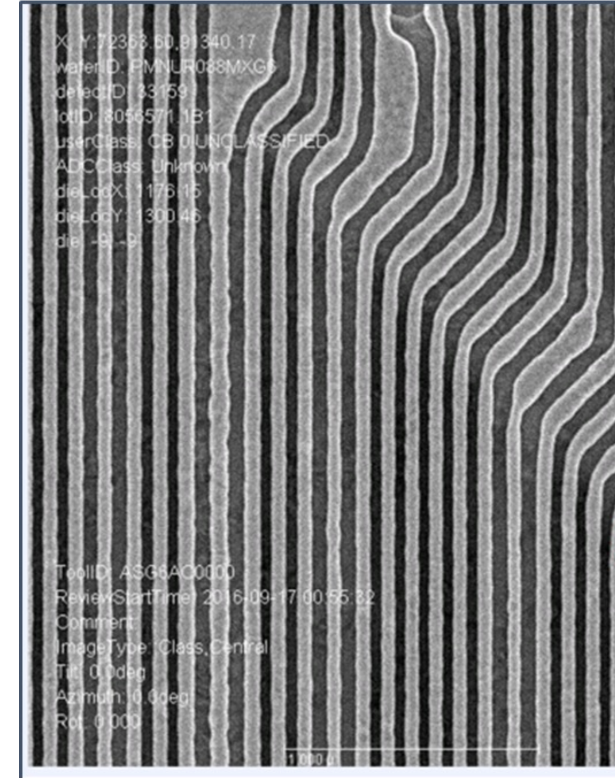
- Device scaling, e.g., CFET
- Library scaling (backside power and other techniques drop track height
- Circuit innovation
- System innovation

So Why Curvy Now?

- Conventional pitch scaling is projected to slow
- Library track height will continue to drop -> increasing congestion
  - C-FET, backside power provide area scaling by dropping tracks
- As metal pitch scales, portion of cross section that is barrier metal increases so there is a natural tendency for resistance/sq to increase
- Reducing wire length, decreasing congestion is a needed technique so we can benefit future innovations (C-FET, library scaling, etc.)

Ezequiel Russell

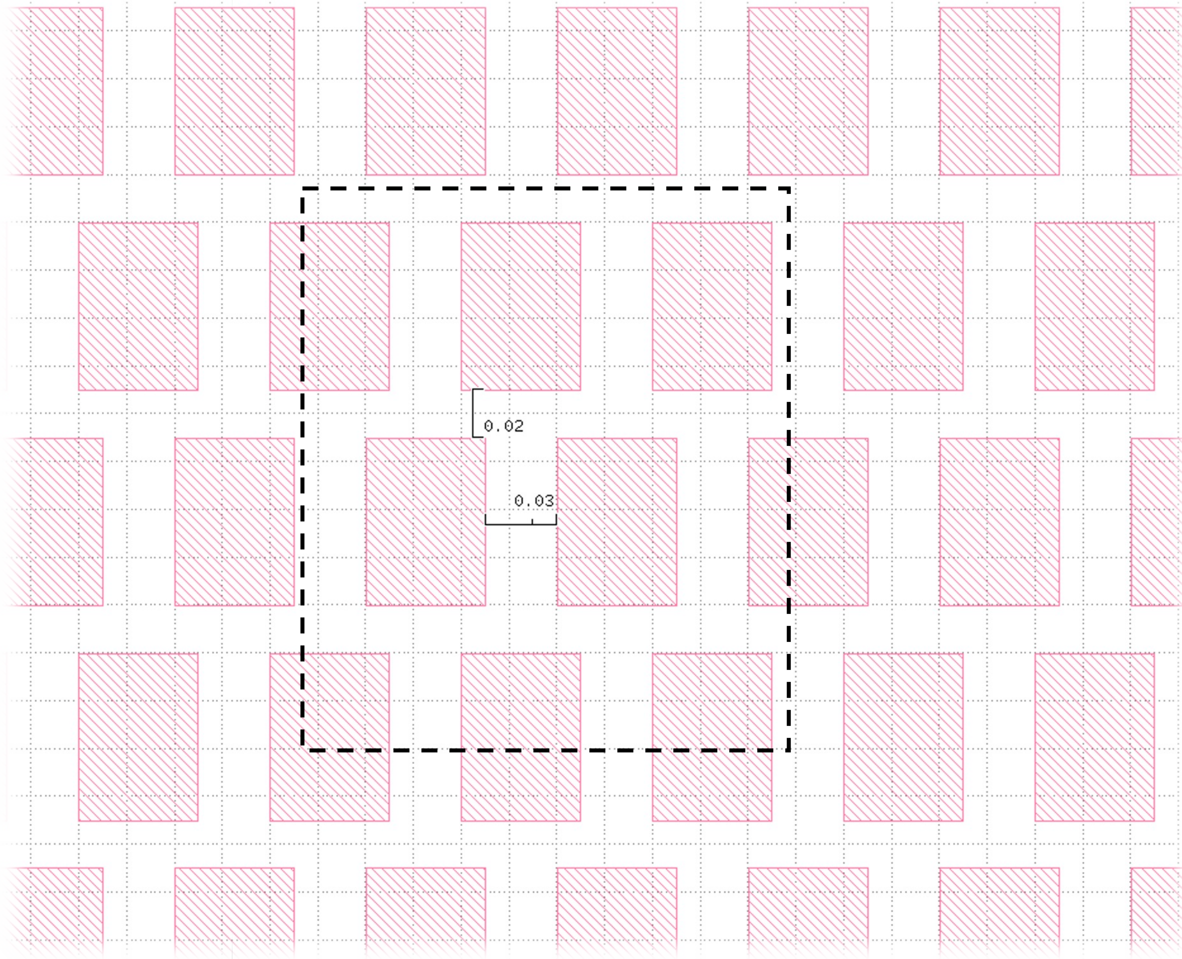
- Senior Director of Mask Technology, Micron Technologies
- Expert in lithography, particularly for DRAM and Flash
- Extensive experience with curvy masks for 193i and EUV

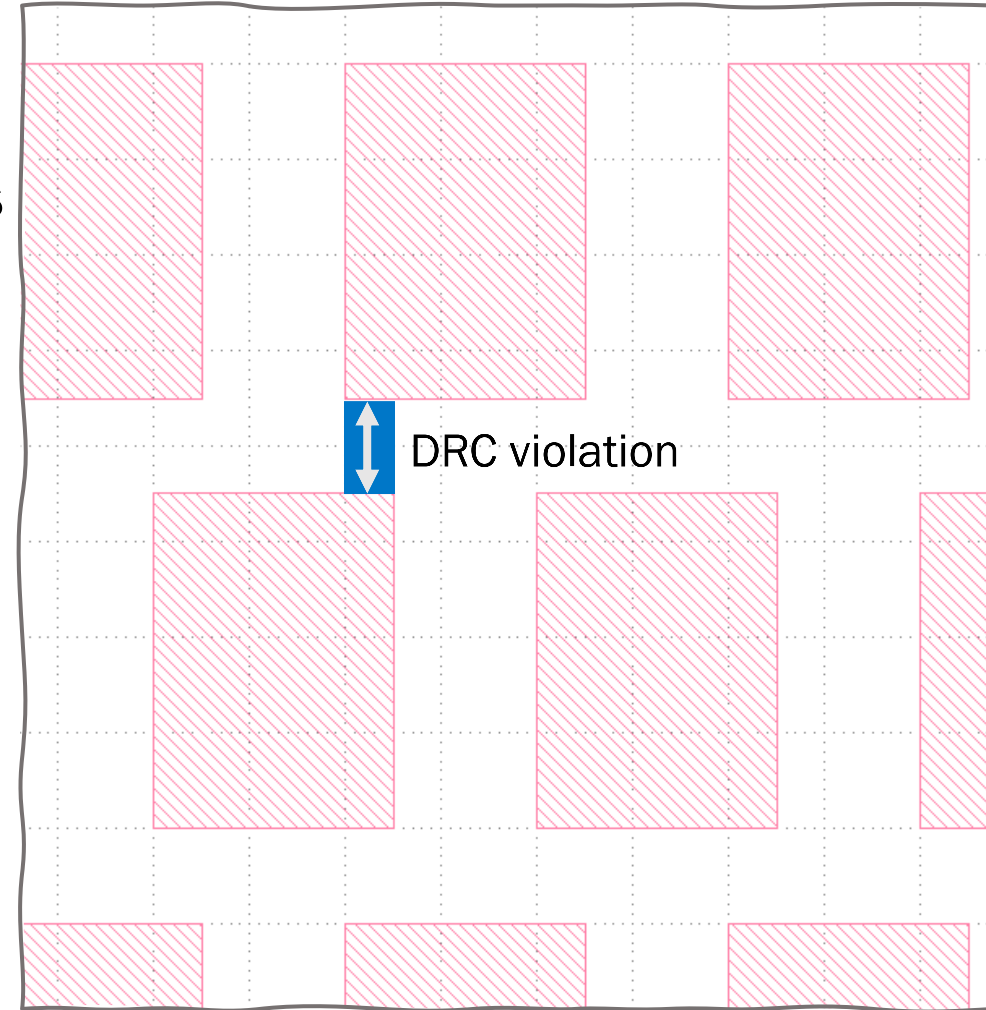


Source: Micron

DRAM Contact Array Case

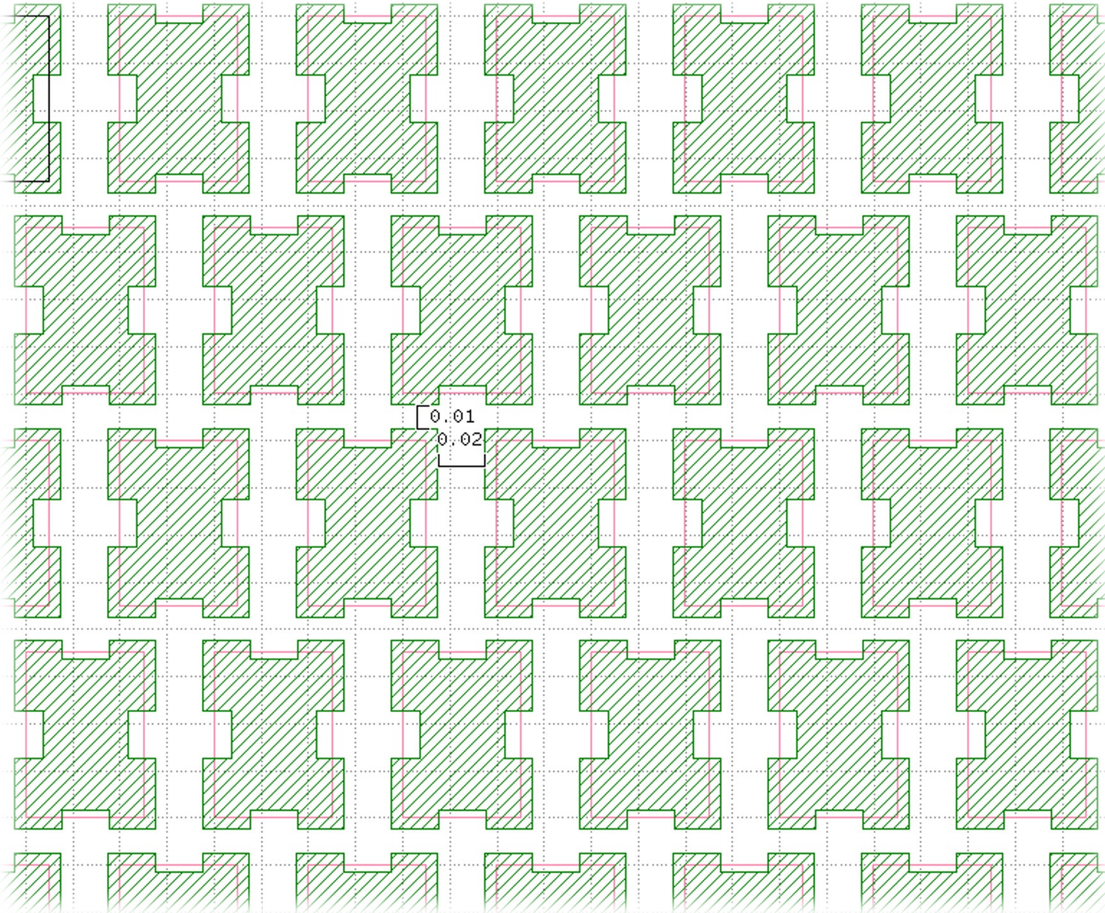
- Manhattan shapes produce countless DRC violations





Source: Micron

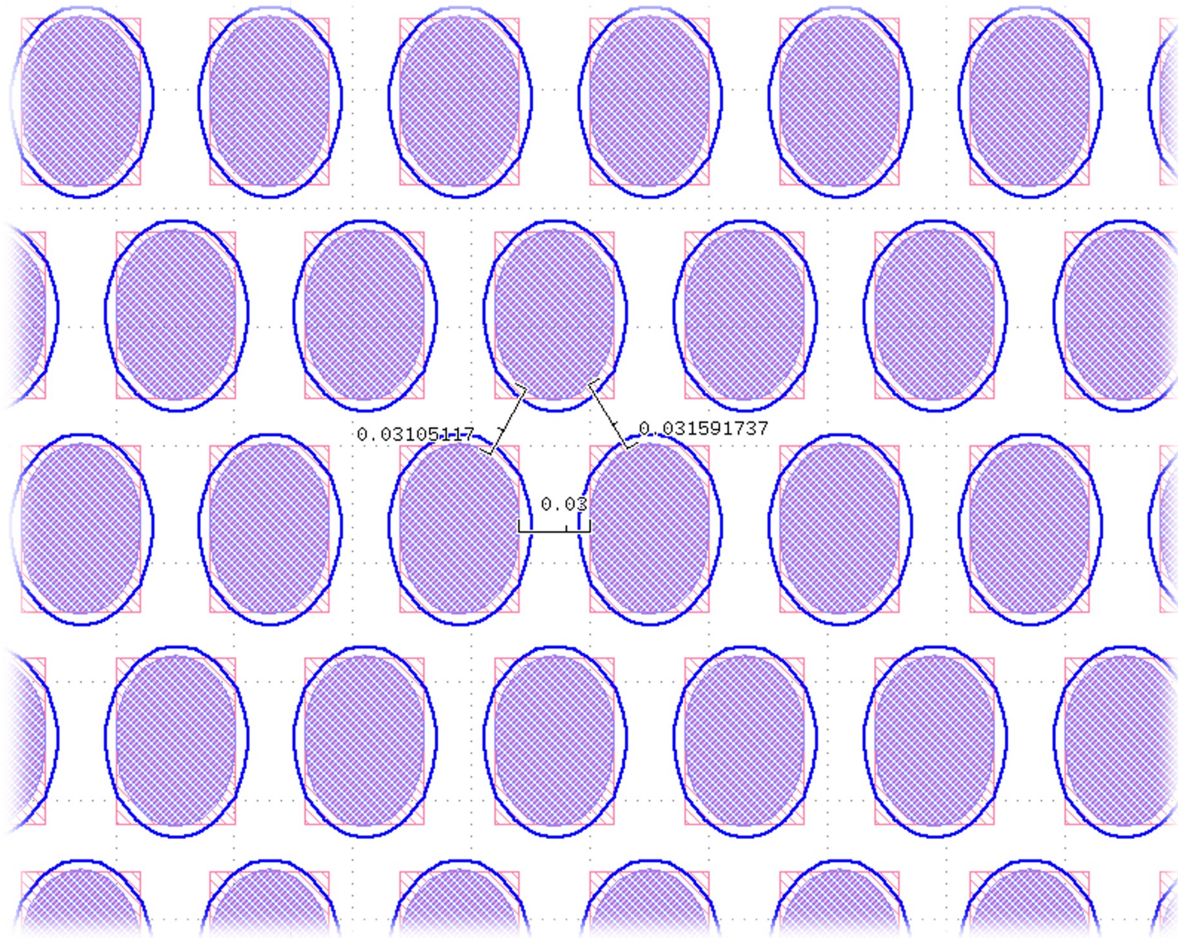
DRAM Contact Array Case



- Post OPC layout
  - Correcting for optical and process effects
- Constrained space for OPC solution
  - MRC violations
- OPC mask shapes are significantly different than wafer printed pattern (Ovals)

Source: Micron

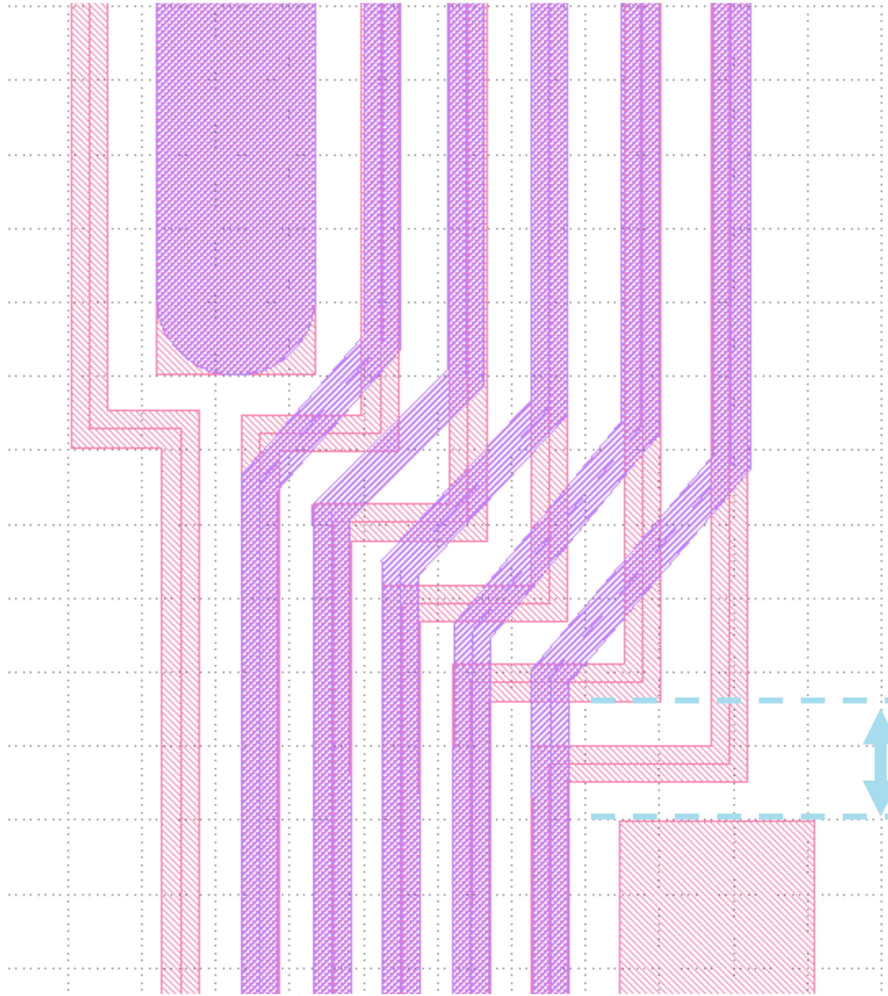
DRAM Contact Array Case



- Curvy target avoids DRC exceptions
- Curvy target facilitates OPC
  - No MRC constraints
  - Less deviation from OPC Mask to wafer shape
- Curvy shapes can be written on mask using state-of-the-art multi-beam writers

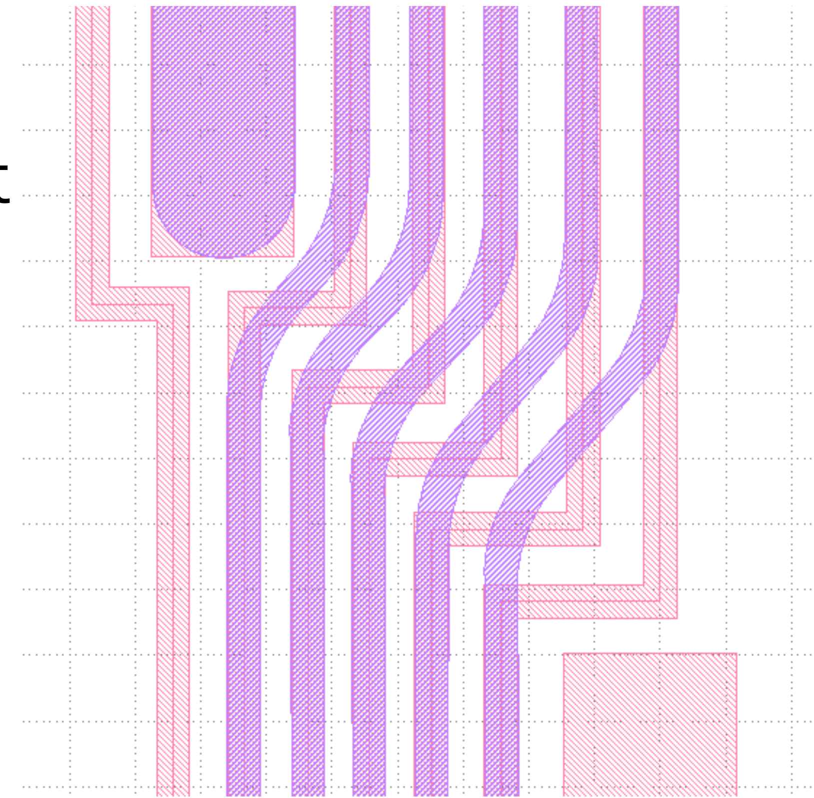
Source: Micron

Metal Routing: Non-Manhattan for Compact Layout



- Leverage 45’s and all-angle to make metal fanouts more compact
- Curvy makes it litho-friendly
  - Less space required between jogs

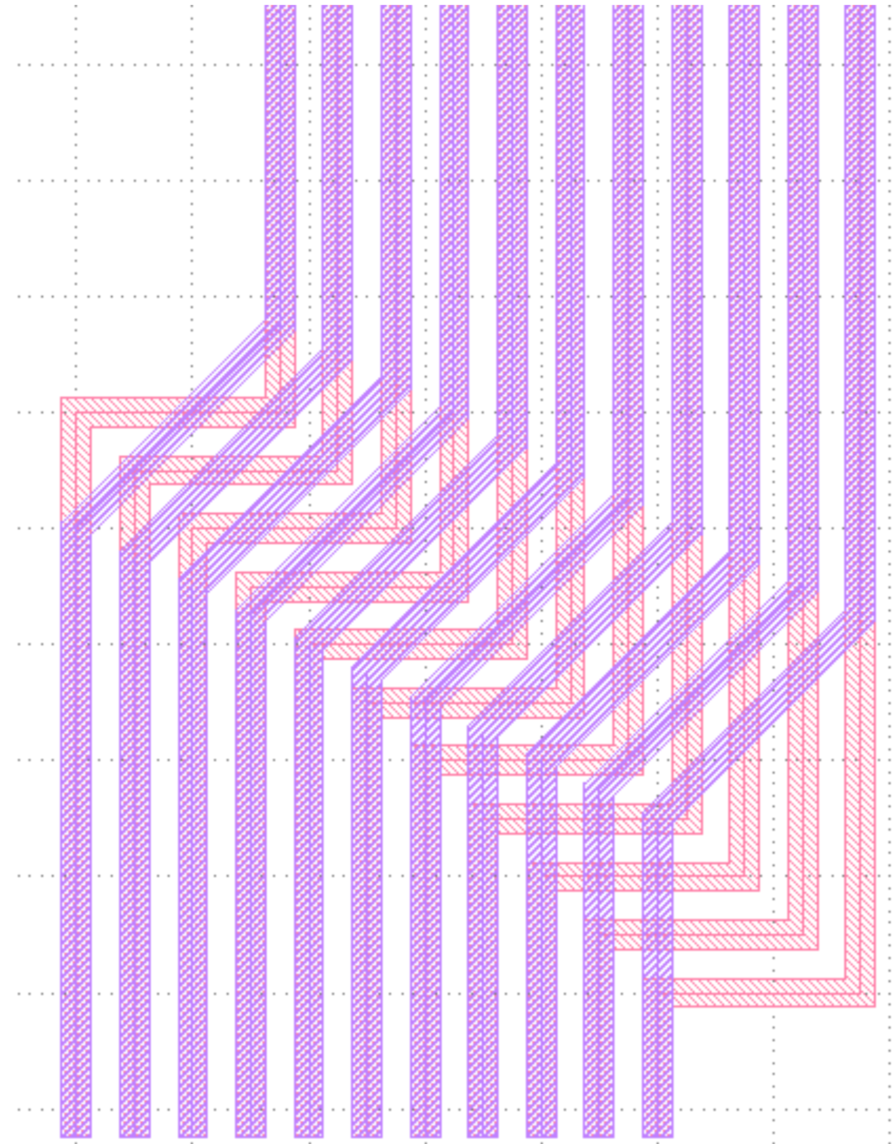
Gained area



Source: Micron

4-Track Jump Example

- 45deg provides more compact layout and shorter routes
- Manhattan jogs will need retargeting to increase width and space, taking an even larger footprint

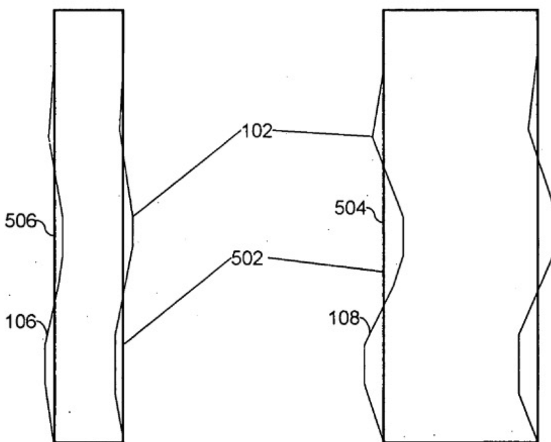


Source: Micron

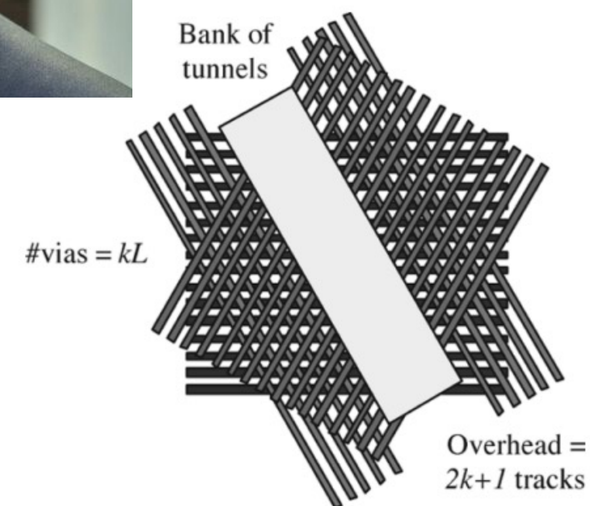
Andrew Kahng

- Professor, UCSD
- Director, OpenROAD Project
- Blaze DFM founder, chairman and CTO

- Extraction-Lithography Connection
- Y Architecture



US Patent 2007/0033558 A1 Nakagawa, Kahng



The Y Architecture for On-Chip Interconnect: Analysis and Methodology, Chen, Cheng, Kahng, et al
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 24, No 4, April 2005

Curvilinear: Perspective

- Curvilinear is *yet* another *potential* **scaling booster** **But ...**
  - **Where and when to insert?** → alternative universes, early lockouts
  - **Chickens and eggs?** → high bar for end-to-end technology, value proofpoints
  - **Expect industry to make business-sensible decisions**
- Past movies in same genre: "X", arguably "DFM", ...
  - **How will the "Curvy" movie be different?**
  - Quest for (cost, value) scaling is more desperate today
  - OTOH, today's audience is much smaller, more consolidated, more risk-averse, ...
- **No question: A new (and mind-blowing!) paradigm for physical structure**

Curvilinear: Thoughts

- **Which IC product organizations are most excited by curvilinear?**
- **What are the top-K limiters?**
  - IP ecosystem
  - Device-layer patterning
  - Alignment, resolution, anisotropy …
  - Row-based standard-cell architecture
  - **+ finite oxygen supply:** backside power, 2.5D/3DHI, … + other uses for 340,000,000x compute!
  - **+ hazy insertion point:** node, layer, die ASP, product PPAC, …
  - **+ stopping points of virtuous cycles:** recapturable die area, density downsides, …
- **What blocks collaborative enablement?**
  - IP moats and unknown cost uplifts
  - Incentives to bring up ecosystem elements (“pioneers get the arrows”)
  - *Can we discuss blockers and unblockers today?*

Steve Teig

- CEO, Perceive
- 2012 Edison, World Technology Awards
- Tangent Over-the-Cell
- X Architecture
- BioCAD, Combichem
- Tabula, Perceive

Vias Are the Enemy

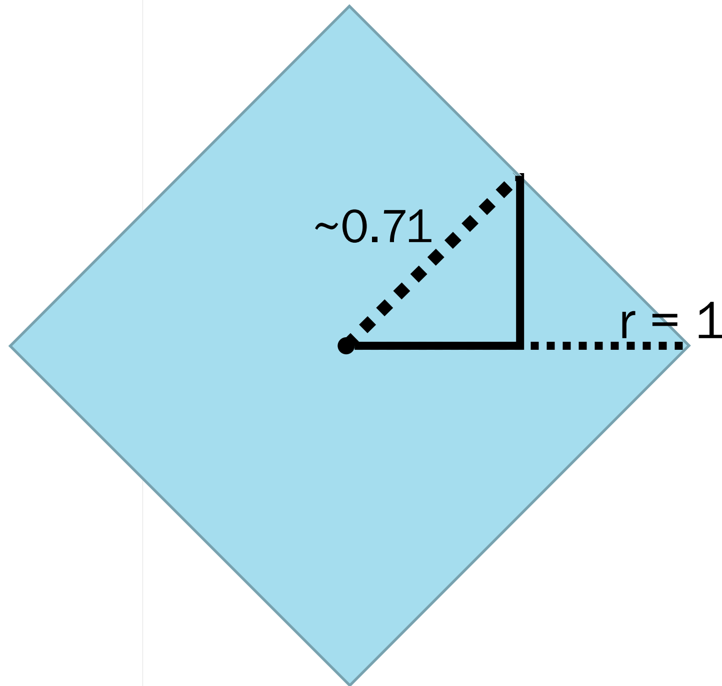
9th Floor
8th Floor
7th Floor
6th Floor
5th Floor
4th Floor
3rd Floor
2nd Floor
1st Floor

Office 1 | Office 2 | Office 3 | Office 4 | Office 5 | Office 6 | Office 7 | Office 8 | Office 9

- Create congestion: pebbles in the stream
- Vias in lower layers are particularly bad
- Manhattan routing almost always needs 2+ vias in lower layers
  - Every turn needs at least 2 vias
  - Added vias come in pairs
- Curvy routing rarely needs any vias for short connections in lower layers
- Vias are physically unreliable
  - Delay has high uncertainty → conservatism
- Reducing vias can reduce wire length a lot!
- Reducing vias can reduce cost

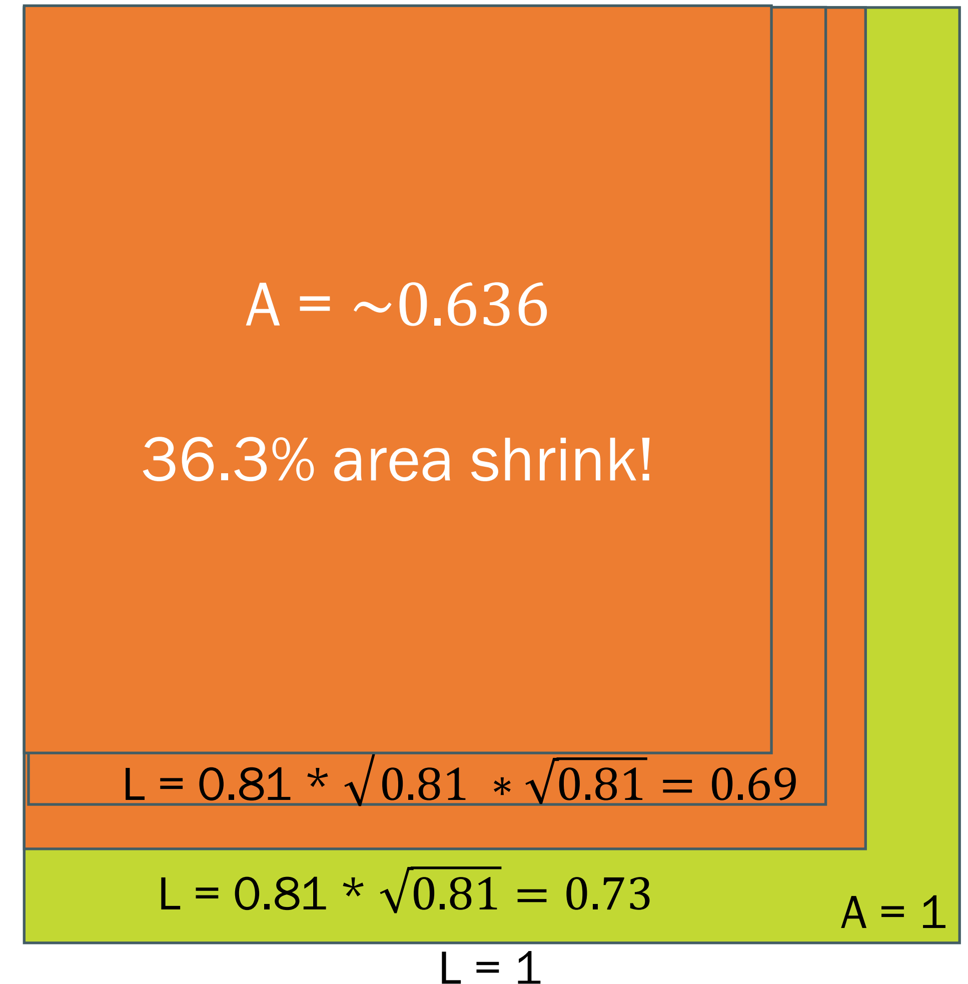
60

Virtuous Cycle: Less Wire = Less Area = Less Wire…



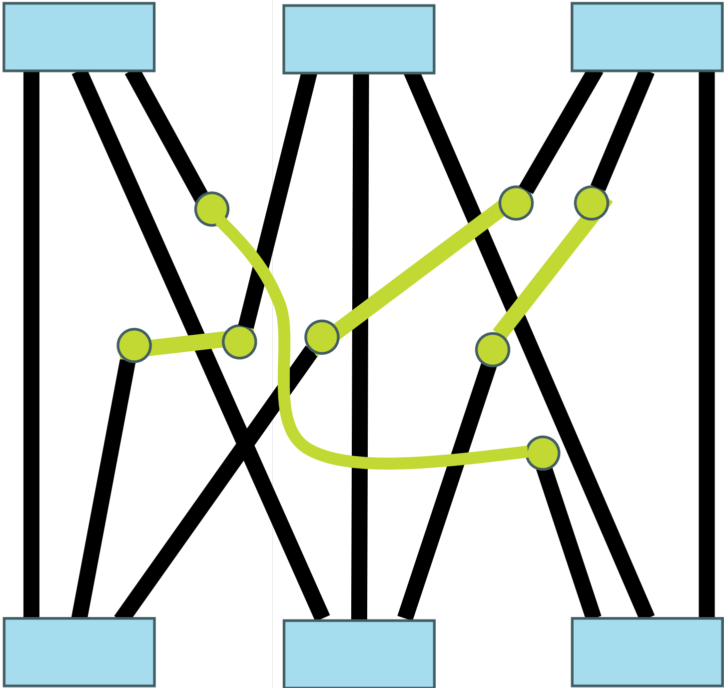
Manhattan placement, curvy (Euclidean) routing:

$$\int_0^1 \sqrt{y^2 + (1-y)^2}\, dy = \frac{2 + \sqrt{2}\ln(1+\sqrt{2})}{4} = \sim\mathbf{0.81}$$

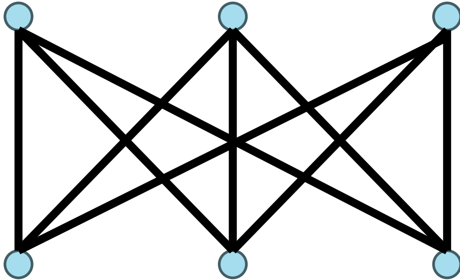


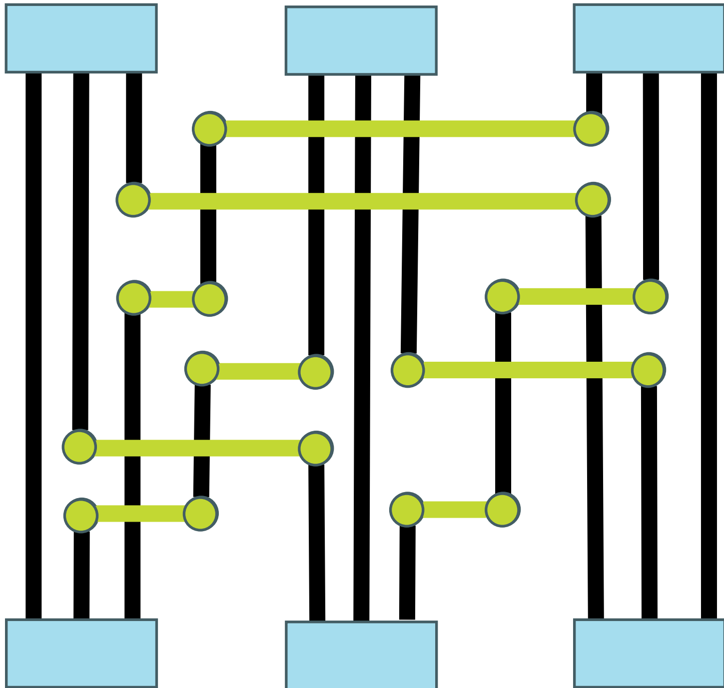
Wirelength is x% smaller → routing area is x% smaller → chip area is x% smaller

Curvy Can Reduce Via Counts by >50%!



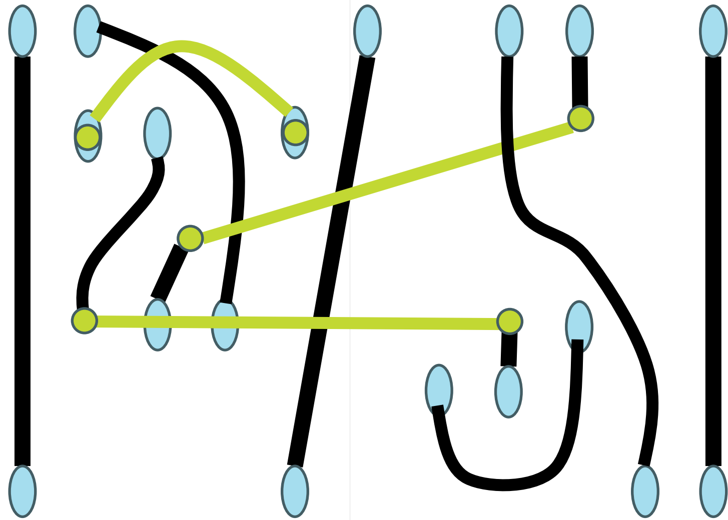
Curvy: 4 via pairs



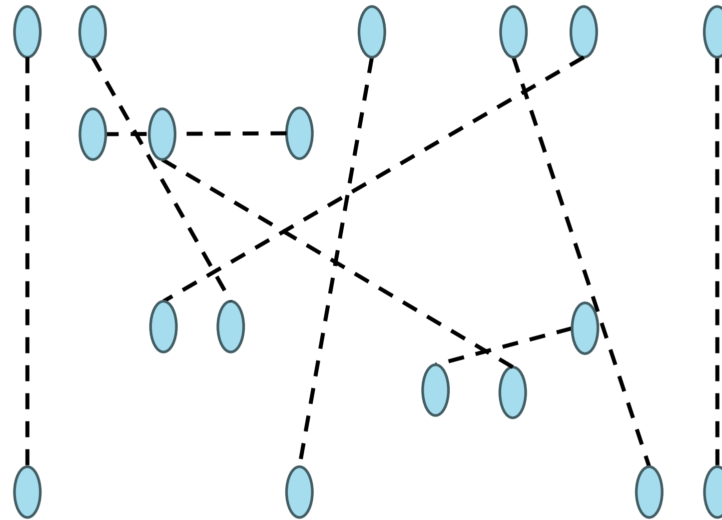


Manhattan: 9 via pairs

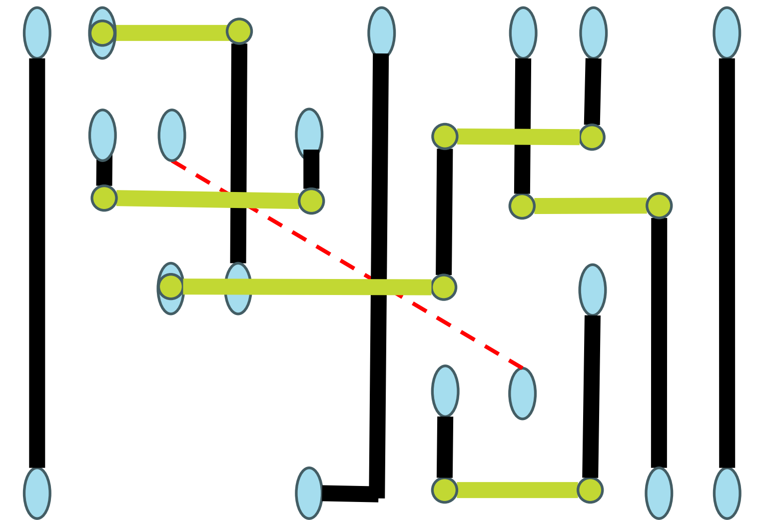
Curvy Can Reduce Via Counts by ~50%!



Curvy: 6 vias



Desired Connectivity
(netlist)

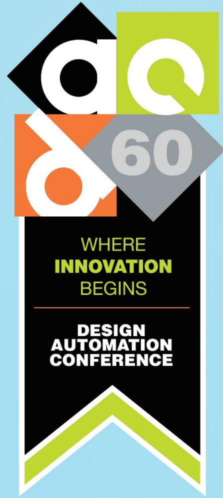


Manhattan: 12 vias and a disconnect

Curvy is a Transformative P&R Technology

- Should reduce wiring area by 33-40% vs. Manhattan
  - Using curvy placement and curvy routing: “virtuous cycle”
- Should reduce via counts by ~50% vs. Manhattan
  - Massively reduces detouring and wiring congestion
  - First-order effect that is not contemplated by simplistic wire length models

- Remove 2 layers of interconnect – maybe even 3 for 9+ signal layers
  - Or reduce die size by 10-15% and remove 1 layer of interconnect
- And reduce performance conservatism (due to manufacturing variability)
  - Which will improve yield, too



Why is Curvy Design an Opportunity Now?

Moderator: Aki Fujimura, CEO, D2S, Inc.

Panel: John Kibarian, CEO, PDF Solutions

Ezequiel Russell, Sr. Director of Mask Technology, Micron

Andrew Kahng, Professor, UCSD

Steve Teig, CEO, Perceive

The Debate on Curvy Design

Barriers

- Fabless needs foundry support
- Foundry needs fabless demand
- Tool infrastructure is way too inefficient for curvy design
- Perception that everything in EDA needs to change
- Benefits are unclear/unproven

- Net: It's a big change

Potential Benefits

- Yield
- Power
- Performance
- Area and layer-pair elimination
- Cost

- Reduce vias and wire length
- EUV and non-EUV leading edge